SCALABLE ARCHITECTURE FOR COMPUTATIONALLY INTENSIVE APPLICATIONS

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ABSTRACT

High Performance Computing Platforms are being used to address operations with complex computational requirements or with significant processing time requirements or requirement to process significant amount of data. With the advent of low cost Field Programmable Gate Arrays (FPGA's), building hardware with parallel architecture for computationally intensive applications has now become possible. FPGA's offer massive and parallel architectures. This paper presents a FPGA based design of parallel architecture which is scalable for hardware implementation of computationally intensive applications. The aim of this work is to design a reconfigurable parallel and scalable High Performance Computing Platform to accelerate computations. The Cryptanalysis of Advanced Encryption Standard (AES) Algorithm is used as a proof of concept.

KEYWORDS: AES, Cryptanalysis, FPGA's, High Performance Computing, Parallel and Scalable Architecture